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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,858	09/22/2003	Yasuo Yamazaki	03500.017567	4328

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
LE, DUNG ANH	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,858	YAMAZAKI, YASUO	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10 and 11* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 9/22/2003 is acceptable.

Drawings

The drawings are objected to for the following reasons.

Figures 6 and 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Set of claims 1- 9

Claims 1- 7 are rejected under 35 USC 102 (e) as being anticipated by Kochi et al. (6,828,085 B2).

Kochi et al. teaches a method for manufacturing a semiconductor apparatus device including a plurality of layers on a semiconductor substrate, said method comprising the steps of:

dividing a pattern of at least a layer into a plurality of sub-patterns; and joining the divided sub-patterns to perform patterning, wherein as to a layer including wiring (col 14, lines 15-30) substantially affecting operation of the semiconductor device10/20 (cokl 5, lines 40-5) depending on a positional relationship to any other wiring, the patterning is performed by one-shot exposure using a single mask (col 14, lines 15-30).

Regarding claim 2, wherein as to a layer including wiring 6/8/12 (figs 2-4) in which a value of parasitic capacitance (col 4, lines 15- 25) generated depending on the positional relationship to any other wiring substantially affects the operation of the semiconductor device, the patterning is performed by one-shot exposure using a single mask (col 14, lines 15-30).

Regarding claim 3, wherein the semiconductor device has a plurality of elements each having a same structure composed of a plurality of layers including a plurality of a same patterns respectively, and as to a layer including wiring which causes dispersion of a characteristic of each of said elements, the dispersion substantially affecting the operation of the semiconductor device, when there are differences in the value of the parasitic capacitance among the elements (col 4, lines 15- 25, the one-shot exposure using a single mask is performed (col 14, lines 15-30).

Regarding claim 4, wherein the semiconductor device further has pixels each including a photoelectric conversion 801 (fig.15) portion, and as to a layer including wiring which causes an output difference (fig. 2) of photoelectric conversion at a degree of being visible in an image, when there are differences in the value of the parasitic capacitance among the pixels, the one-shot exposure using a single mask is performed. (col 14, lines 15-30).

Regarding claim 5, the method further comprising the step of forming each of the pixels and/or a peripheral circuit by means of a CMOS process (col 5, line

25-30), wherein control wiring of a field effect transistor in the pixel is formed by the one-shot exposure using a single mask. (col 14, lines 15-30).

Regarding claim 6, wherein wiring directly connected to the semiconductor substrate is formed by the one-shot exposure using a single mask. (col 14, lines 15-30).

Regarding claim 7, wherein the wiring is made of polysilicon (col 5, line 20-25).

Set of claims 10- 11

Claims 10- 11 are rejected under 35 USC 102 (e) as being anticipated by Kochi et al. (6,828,085 B2).

Kochi et al. teach a method for manufacturing a semiconductor apparatus device, said method including the steps of dividing a pattern of at least one layer into a plurality of sub-patterns, and joining the divided sub-patterns to perform patterning, said method comprising the steps of:

forming source and drain regions of a MOS transistor on a semiconductor substrate; forming a gate insulating film and a gate electrode of the MOS

transistor; forming a wiring layer including gate wiring connected to the gate electrode (figs 2-3; col5, lines 1-40); and

forming the gate wiring by performing patterning by means of a one-shot exposure to the wiring layer (col 14, lines15-30).

Regarding claim 11, the method further comprising the step of forming a photoelectric conversion portion 801(col 9, line 3; fig. 15).

Reasons for Indication of Allowable Subject Matter

Claims 8 and 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. **Kochi et al. (6,828,085 B2) and Background of Invention**, taken individually or in combination, do not teach the claimed invention having **(Regarding claim 8),** wherein only as to the layer including the wiring substantially affecting the operation of the semiconductor device depending on the positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers, the patterning is performed by division exposure and **(Regarding claim 9)** the layers to be patterned prior to the patterning of the layer

including the wiring substantially affecting the operation of the semiconductor device depending on positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers to be patterned after the one-shot exposure, the patterning is performed by division exposure.

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818